application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, or the following detailed description.

[0020] For simplicity and clarity of illustration, the drawing figures illustrate the general manner of construction, and descriptions and details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the invention. Additionally, elements in the drawings figures are not necessarily drawn to scale. For example, the dimensions of some of the elements or regions in the figures may be exaggerated relative to other elements or regions to help improve understanding of embodiments of the invention.

[0021] The terms "first," "second," "third," "fourth" and the like in the description and the claims, if any, may be used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in sequences other than those illustrated or otherwise described herein. Furthermore, the terms "comprise," "include," "have" and any variations thereof, are intended to cover non-exclusive inclusions, such that a process, method, article, or apparatus that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. The term "coupled," as used herein, is defined as directly or indirectly connected in an electrical or non-electrical manner. As used herein the terms "substantial" and "substantially" mean sufficient to accomplish the stated purpose in a practical manner and that minor imperfections, if any, are not significant for the stated purpose.

[0022] As used herein, the term "semiconductor" is intended to include any semiconductor whether single crystal, poly-crystalline or amorphous and to include type IV semiconductors, non-type IV semiconductors, compound semiconductors as well as organic and inorganic semiconductors. Further, the terms "substrate" and "semiconductor substrate" are intended to include single crystal structures, polycrystalline structures, amorphous structures, thin film structures, layered structures as for example and not intended to be limiting, semiconductor-on-insulator (SOI) structures, and combinations thereof The term "semiconductor" is abbreviated as "SC." For convenience of explanation and not intended to be limiting, semiconductor devices and methods of fabrication are described herein for silicon semiconductors but persons of skill in the art will understand that other semiconductor materials may also be used. Additionally, various device types and/or doped SC regions may be identified as being of N type or P type, but this is merely for convenience of description and not intended to be limiting, and such identification may be replaced by the more general description of being of a "first conductivity type" or a "second, opposite conductivity type" where the first type may be either N or P type and the second type then is either P or N type.

[0023] In order to be able to build ESD devices that have different Vt**1** values to meet the protection needs of different core circuits **24** see FIG. **1**), it is common to design ESD devices such that Vt**1** depends upon the spacing of a particular device dimension. For example, bipolar transistor **25** of FIG. **2** is often a lateral transistor wherein Vt**1** depends upon a base-collector spacing dimension D. Transistor **40** of FIG. **4** (described below) illustrates a lateral transistor having base-collector spacing dimension D. One of the difficulties of using bipolar transistors such as bipolar transistor **25**, **40** in ESD applications is that there can be significant variation AD in base-collector spacing dimension D across a SC wafer and/or SC die as a function, for example, of the azimuthal orientation of transistor **25**, **40** on the wafer or die. In addition, the spacing dimension D can have significant variation ΔD from one wafer to another, e.g. between manufacturing different lots. This has the result that Vt**1** of nominally identical devices can be different in different regions of the same IC and from manufacturing lot to manufacturing lot, depending, for example, on their relative azimuthal orientation on the IC die or wafer. This Vt**1** variation can adversely affect overall manufacturing yield and is not desirable. Various process modifications may be used to minimize such effect, but such modifications are often accompanied by an undesirable increase in manufacturing cost or other difficulties. The Vt**1** variation can become especially acute when such ESD clamp transistors are cascaded, that is, serially coupled in stacks in order to obtain higher vales of Vt**1** than can be provided by single ESD clamp transistor **25**, **40**.

[0024] There is an ongoing need to provide improved ESD clamps that operate at more consistent trigger voltages Vt**1** independent of their location or orientation on a particular IC, especially stacks of ESD clamps adapted to provide higher values of Vt**1** than can be obtained with single ESD transistor **25**. Further, it is desirable that the improved ESD clamps be obtainable without significant modification of the manufacturing process used for forming the clamps and the associated circuit core of the IC. Furthermore, other desirable features and characteristics of the present invention will become apparent from this detailed description of the invention and the appended claims herein, taken in conjunction with the accompanying drawings and the background of the invention.

[0025] FIG. **4** shows a simplified cross-sectional view of ESD clamp transistor **40**, **70** implemented in semiconductor substrate **72** according to an embodiment of the present invention. Transistor **40**, **70** fulfills the function of transistor **25** in FIG. **2** and ESD clamp **21** in FIG. **1**. Transistor **40**, **70** is formed in substrate **72** (e.g. P) having upper surface **71** and with N type buried layer (NBL) region **73** therein. Overlying NBL **73** is region **74** (e.g., P) extending from NBL **73** to surface **71** and within which are formed shallow trench isolation (STI) regions **79**, deep trench isolation (DTI) regions **792**, N WELL regions **761**, **762** (collectively **76**) with contact region **80** (e.g., N+) and P WELL region **75**. Doped contact region **77** (e.g., P+) is provided in P WELL region **75** to make Ohmic contact to P WELL region **75**. P WELL region **75** is generally somewhat more heavily doped than P region **74**. Doped region **78** (e.g., N+) in P WELL region **75** serves as the emitter, P WELL region **75** (with portion **85** of P region **74**) serves as the base, and N WELL region **762** with N+ contact region **80** serves as the collector of transistor **40**, **70**. Dielectric layer **81** is conveniently provided on surface **71** with openings therein extending to base contact region **77**, emitter region **78** and collector contact region **80**. Conductor **82** makes Ohmic contact to collector contact region **80**, and conductor **83** makes Ohmic contact to base contact region **77** and emitter region **78**, connecting regions **77**, **78** together. Conductor **82** of transistor **40**, **70** is conveniently coupled to terminal **22** and conductor **83** of transistor **40**, **70** is conveniently coupled to terminal **23** of ESD circuit **20**. Further N region **86** is provided in Ohmic contact with N WELL region